III / II Sem CSE

Code No: 09A60502 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B. Tech III Year II Semester Examinations, June-2014
VLSI Design
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1. With neat sketch explain fabrication process of Twin well CMOS Processes.

2.a) Derive an equation for I_{ds} of an n channel enhancement MOSFET operating in saturation region

b) An nMOS transistor is operating in saturation region with the following parameters.Vgs=5V, Vtn =1.2V, (W/L) =10, $\mu_n c_{ox}$=110μA/V^2. Find transconductance of the device.

3. Draw the circuit and layout diagram for three input AND-OR-INVERT CMOS gate.

4.a) Discuss about area capacitances of MOS layers and give area capacitance calculations with suitable examples.

b) Explain the properties of pass transistors.

5. Draw the circuit diagram for 4 × 4 barrel shifter using complementary transmission gates and explain its shifting operation.

6.a) Design a 4 × 4 ROM and explain its operation.

b) Write short notes on context addressable memory.

7.a) What are the advantages of standard cell designs compared to gate arrays. What are the fundamental components of standard cell?

b) Discuss the parameters influencing low power design.

8.a) Explain the need for testing. Explain the design strategies for test.

b) Explain about various system level test techniques.

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